

REMARKS/ARGUMENTS

Claims 1, 2 and 7-13 are currently pending. No claims have been amended. No new claims have been added. Reconsideration of the application is respectfully requested in light of the following remarks.

Claim Rejections - 35 U.S.C. § 03(a)

Claims 1-2 and 7-13

Claims 1-2 and 7-13 have been rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Lee et al. (U.S. Patent No. 6,820,158) in view of Kaganoi (U.S. Patent No. 6,772,269), and further in view of Vanbrabant et al. (U.S. Patent No. 4,679,192). Applicants respectfully traverse the rejection in view of the comments below.

Page 12 of the Office Action states that Applicants' arguments in their October 12, 2007 reply are now moot in view of new grounds of rejection based on the Vanbrabant reference. The Office Action further states that: (1) Vanbrabant teaches the bus control module provided with a counter that counts the pulses between the passage of two arbitration frames relayed on the data bus (Vanbrabant, col. 4, lines 51-65), and (2) Vanbrabant monitors the passage of an arbitration frame by a bus control module by ENAB feature in such a way that the pulses between two passages of the arbitration are counted and wherein a new arbitration frame having a deactivated bit is transmitted by the control module when the number of counted pulses exceeds a predetermined value (Vanbrabant, col. 2, line 60 to col. 3, line 15).

Applicants respectfully submit that Vanbrabant does not overcome deficiencies of Lee and Kaganoi for the reasons stated below.

(1) Vanbrabant's disclosure of the bus control module provided with a counter that counts the pulses between the passage of two arbitration frames relayed on the data bus

Vanbrabant teaches an apparatus for data transmission having several stations (S_1, S_2, \dots, S_n) for transmitting digital signal[s?] from one station to another and a main station MS with a clock pulse generator CLK. Stations S_1 - S_n and main station MS have access to data bus B.

Vanbrabant further discloses: "To avoid mixing of data the communication path B, and, more specifically [sic], the data channel is assigned to one station at a time." (col. 2, lines 36-38). Each station S_1 - S_n is equipped with an address register ADDR with a unique value. (col. 2, lines 48-49). The clocking of Main Station's clock CLK increments a counter CNTR on the data bus B. When the value of the counter CNTR matches the address value ADDR for station S_i , that station is given access to bus B. To prevent clock pulses CLK from further incrementing counter CNTR on bus B, station S_i blocks the access of counter CNTR to Main Station's clock CLK by asserting a SEND-signal on bus B (col. 3, lines 8-15). Notice that for as long as CNTR value is equal to a specific station's (i.e. S_i 's) ADDR value, that station will be the only one with the access to data bus B, because a station can only send data to bus B when the value of counter CNTR corresponds to that station's ADDR value.

Thus, when station S_i gets the access to the bus, and blocks CNTR from advancing by asserting SEND signal, that particular station can retain control of bus B for unlimited time, to the exclusion of all other stations. Vanbrabant discloses what happens when station S_i completes the data transfer: "At the end of the transmission of data from one station to the other, the transmission station no longer transmits data and [...] the SEND-signal is switched of [sic]." (col. 3, lines 14-17). Switching SEND-signal off will, in turn, enable Main Station's clock CLK to again start incrementing counter CNTR on the data bus. As CNTR value increments up, the new value of counter CNTR will match address ADDR of station S_{i+1} , which will now get the control, stop counter CNTR by asserting SEND-signal, transmit data, and restart counter CNTR by turning off SEND-signal. Next, counter CNTR increments again, and station S_{i+2} gets the control over the data bus, and so on.

The above-summarized disclosure of Vanbrabant is in stark contrast to what is required by presently pending claims 1 and 13, where any of the Client Application Modules (the closest equivalent to station S_i of Vanbrabant) can request access to the data bus through any of the Host Device (the closest equivalent to main station MS of Vanbrabant). Next, the bus control module of the presently pending claims verifies whether the data bus is already busy or is available by finding the value of the activity bit on the data bus (see, e.g., step 104 on Fig. 2). If

the activity bit is not set, meaning that the data bus is available, the bus control module allows data on the bus, while also setting the activity bit, thus signaling to other client devices that the data bus is presently not available to them (see, e.g., the first full paragraph on page 7). Thus, any client application module may request access to the data bus at any given time. The client application modules of presently pending claims do not need to wait for their turn, as in Vanbrabant where any station can send data only if its ADDR value corresponds to COUNT value on the bus. In the presently pending claims, for as long as the data bus is available, i.e. activity bit is not set, the bus control module will allow the access for a requesting client device. Vanbrabant has no disclosure or suggestion of this "out of turn" access to the data bus by its stations. Furthermore, Vanbrabant does not disclose or suggest a counter that "count[s] the pulses between the passage of two arbitration frames relayed on the data bus," as required by claims 1 and 13.

(2) Vanbrabant's disclosure that a deactivated bit is transmitted by the control module when the number of counted pulses exceeds a predetermined value (i.e. a reset function)

The operation of Vanbrabant's "reset function" is explained in col. 3, lines 32-40 of its disclosure: "For the case in which 256 stations are connected to the common communication path B and one of the numbers between 1 and 256 [the ADDR numbers - comment by the undersigned] is assigned to each station, the counters CNTR are reset after 256 consecutive clock pulses and a new cycle starts." (col. 3, lines 36-40). Thus, Vanbrabant's "reset function" invariably occurs after all the stations S_1 - S_n had their turn to transmit data to the bus. After the reset, a new access cycle starts for stations S_1 - S_n . The "reset" in Vanbrabant is not a consequence of an abnormal event, but, instead, happens normally after each station had its serial turn at the data bus. Vanbrabant cannot get back to the normal operation if any of its stations hangs-up. Instead, Vanbrabant's station S_i keeps the data bus blocked for an unlimited time if the station failure occurs. A hardware reset is needed to get the system back to normal operation.

In stark contrast to Vanbrabant's reset function, presently pending claims 1 and 13 define that: "the bus control module transmits a new arbitration frame having a deactivated activity bit in order to release the blocked data bus." The release of the blocked data bus occurs

when: "the number of said elapsed pulses exceeds said predetermined target number." Thus, deactivation of the blocked data bus in the presently pending claims occurs after the data transfer took an unexpectedly long time, which is a failure condition that typically indicates that the bus is hung-up. The bus control module uses the reset function to recover after a failure of data transmission, as explained in the first full paragraph on page 8 of the Application as filed:

The bus control module BCM 8 monitors the data bus 9 in that it counts the pulses between the passage of two arbitration frames using a counter. If the count exceeds the predetermined limiting value of the number of pulses per access [...] the bus control module 8 retransmits an arbitration frame having a deactivated activity bit and thus automatically releases the blocked data bus 9 again.

There is no disclosure or suggestion of this additional recovery feature of the data bus in Vanbrabant.

(3) The rejection of the claims for obviousness over Lee and Kaganoi in view of Vanbrabant

The Office Action asserts that Lee teaches a device for data communication having, inter alia, the transmission path implemented as a data bus and an arbitration unit that decides which master may use the ring when data communication conflicts arise. (Column 5, lines 40-56). However, Lee's arbitration unit is provided decentrally, outside of the data bus connecting Master to Target (Lee, Figs. 4A or 4B). The arbitration unit of Lee thus communicates independently from the bus, and, consequently, needs additional signal lines which are specifically dedicated to the arbitration unit. In the presently pending claims, the bus control module, which the Office Action roughly compares to Lee's arbitration unit, is located on the data bus 9, thereby being an integral part of the ring connector transmission path that connects Master and Client interface modules. The bus control module placement of the presently pending claims does not require additional signal lines for the bus control module.

The Office Action alleges that it would have been obvious to one of ordinary skill in the art to use the bus switch bridge of Kaganoi (col. 3, lines 1-3) in the system of Lee to increase the transfer bandwidth of the sources. Applicants respectfully submit that it is not obvious to combine the system of Lee, in particular Lee's arbitration unit, with the bus switch

bridge of Kaganoi, because with the presently pending claims a person having ordinary skill in the art would seek to improve on the arbitration between two frames. Thus, a combination of the Kaganoi and Lee references with a purpose to, according to the Office Action, "increase the transfer bandwidth of the sources" is not contemplated by a person skilled in the art.

Nevertheless, assuming *arguendo* that a motivation to combine exists, which does not, Applicants respectfully submit that to combine the arbitration unit of Lee with the bus switch bridge of Kaganoi would lead to an illogical end result. In the presently pending claims, a person skilled in the art would not seek an increase in the transfer bandwidth of the sources, because one of the goals of the presently pending claims is to achieve error-free arbitration frame transmission at the expense of the transfer bandwidth, since the arbitration frames in the presently pending claims are re-transmitted as needed to assure proper detection by the client (page 9, cols. 8-11). Thus, a person skilled in the art would, in fact, attempt to exclude the arbitration unit of Lee from the presently pending claims in order not to compromise the desired accuracy of the device over the unnecessary increase in bandwidth.

Next, Applicants respectfully submit that even if the arbitration unit of Lee were hypothetically combined with the bus switch bridge of Kaganoi, the end result would differ from the presently pending claims. The hypothetical combination of Kaganoi and Lee, as suggested by the Office Action, would be based on the Kaganoi device, which allows sending new frames on the bus. In this hypothetical combination, the transmission speed along the bus is not limited by the inability of each module along the bus to keep up with the data transfer amount (col. 3, lines 6-8 and 56-58). The Kaganoi device can afford this transfer speed increase, because that device has a number of input and output registers which serve as temporary storing buffers for the data missed by the modules (col. 3, lines 26-33). Synchronization in the time domain is not achieved (neither it is needed, thanks to the buffers) in the device of Kaganoi. The hypothetical combination of Kaganoi and Lee, as suggested by the Office Action, would generate fast, but unsynchronized, frames on the data transmission bus. Inevitably, the lack of synchronization would lead to the events where more than one arbitration frame is generated simultaneously, which would generate errors and confuse the bus communication of the presently pending

claims, thereby obliterating the essential function of the device in presently pending claims 1 and 13. Therefore, Applicants respectfully submit that presently pending claims 1 and 13 are not obvious over Lee in view of Kaganoi.

Accordingly, Applicants respectfully submit that presently pending claims 1 and 13 are not obvious over Lee in view of Kaganoi, and further in view of Vanbrabant.

Claim 2

Claim 2 has been rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Lee, in view of Kaganoi, in further view of Vanbrabant, and further in view of Chang (U.S. Patent No. 4,679,192).

Dependent claim 2 includes all of the features and elements of its basis claim 1, which is non-obvious over Lee, in view of Kaganoi, in further view of Vanbrabant, as explained in detail above. Therefore, Applicants submit that dependent claim 2 is also patentable at least because it depends from its patentable parent claim 1.

Claims 10-12

Claims 10-12 have been rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Lee, in view of Kaganoi, in further view of Vanbrabant, and further in view of Chang and in further view of Jhang (U.S. Patent No. 6,253,292).

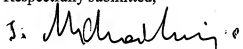
Dependent claims 10-12 include all of the features and elements of their basis claim 1. Therefore, Applicants submit that dependent claims 10-12 are also patentable at least because they depend from their patentable parent claim 1.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (415) 273-4317 (direct dial).

Respectfully submitted,



Dr. Jadran (Adrian) Mihailovic
Reg. No. 57,874

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
Attachments
JM:lrj
61325964_1.DOC